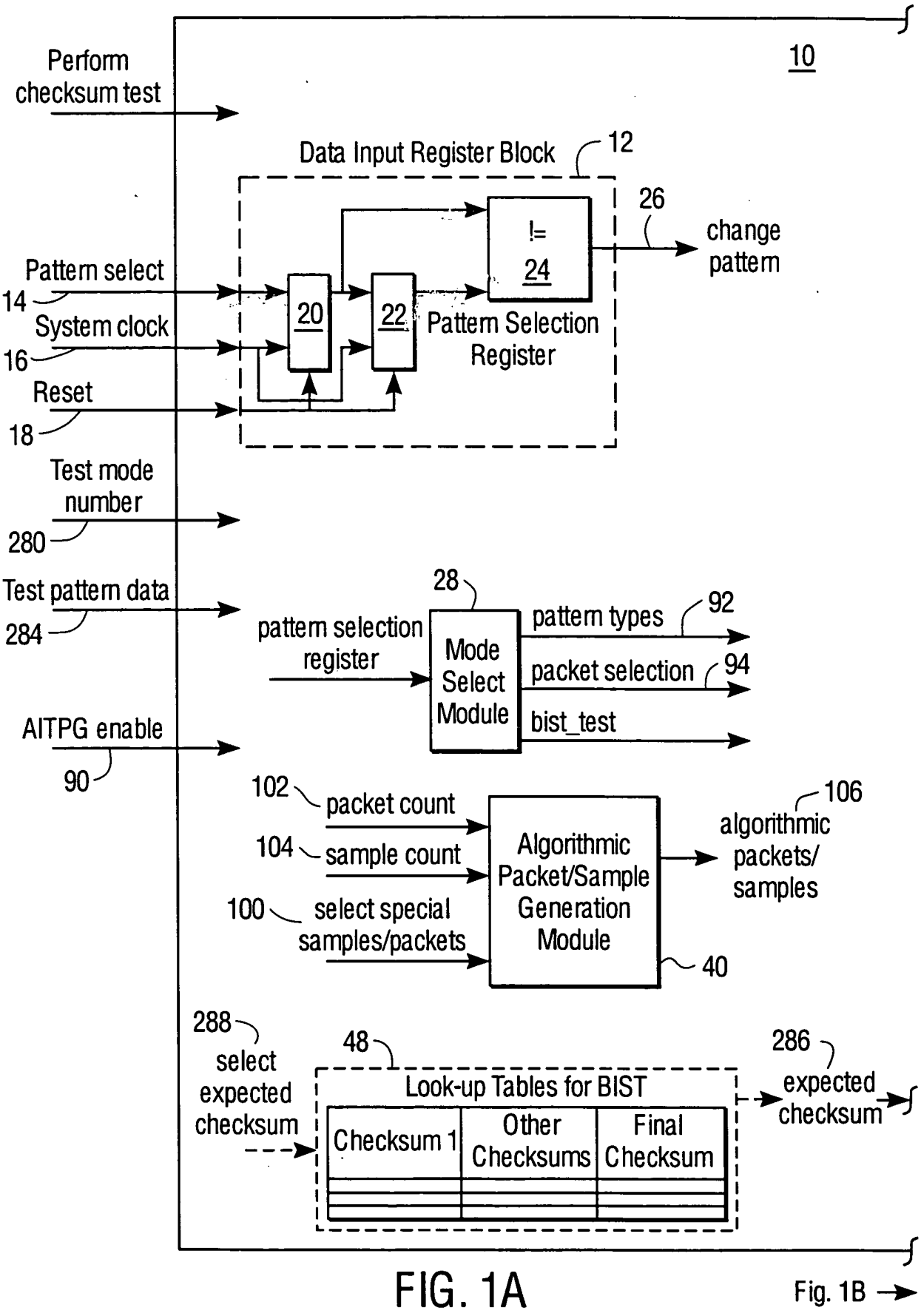
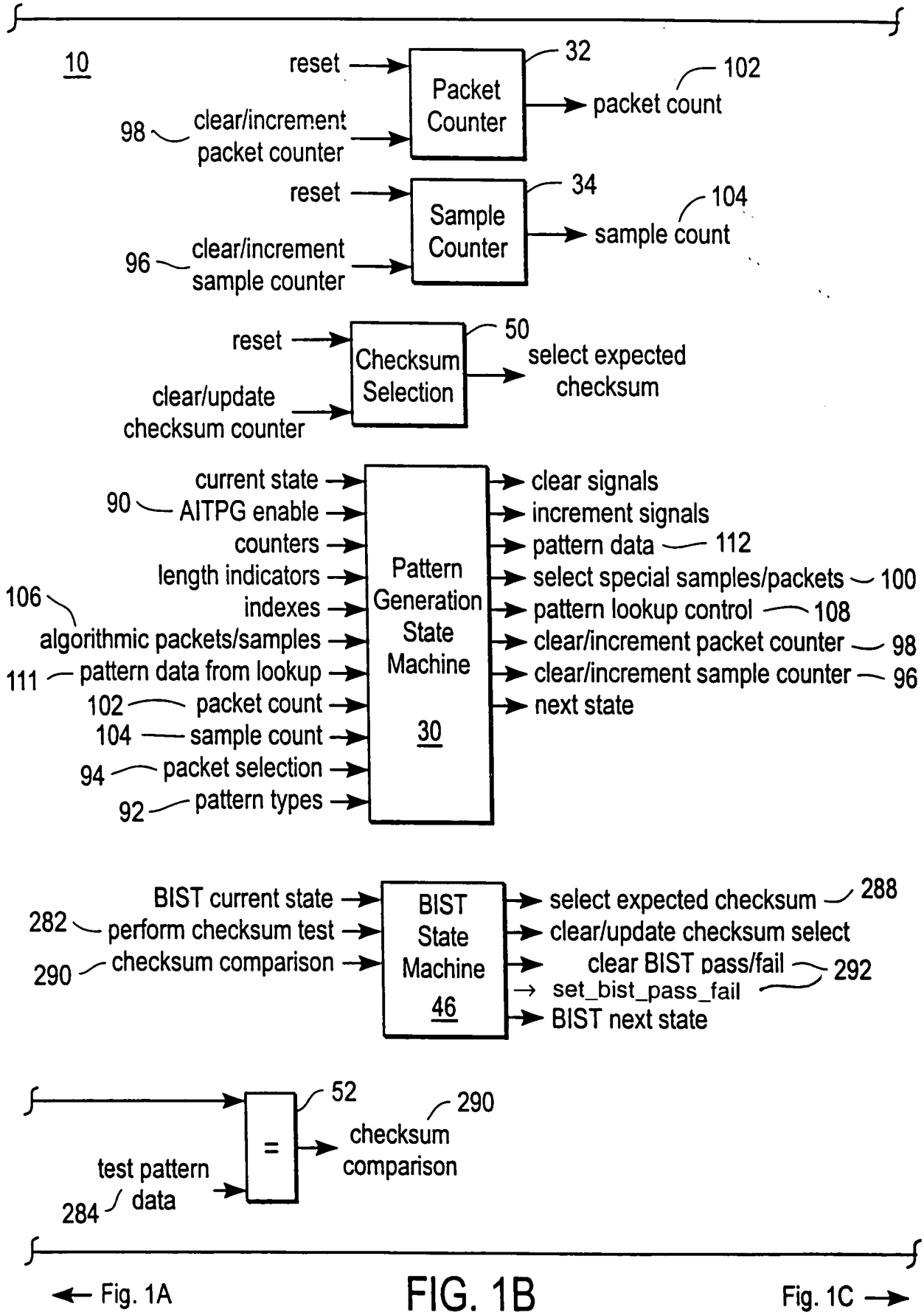

10
Perform checksum test
Data Input Register Block
12
26
change pattern
!=
24
Pattern select
14
System clock
16
Reset
18
20
22
Pattern Selection Register
Test mode number
280
Test pattern data
284
28
pattern selection register
Mode Select Module
pattern types
92
packet selection
94
bist_test
AITPG enable
90
102
packet count
104
sample count
100
select special samples/packets
Algorithmic Packet/Sample Generation Module
40
106
algorithmic packets/ samples
288
select expected checksum
48
Look-up Tables for BIST
Checksum 1
Other Checksums
Final Checksum
286
expected checksum
Fig. 1B

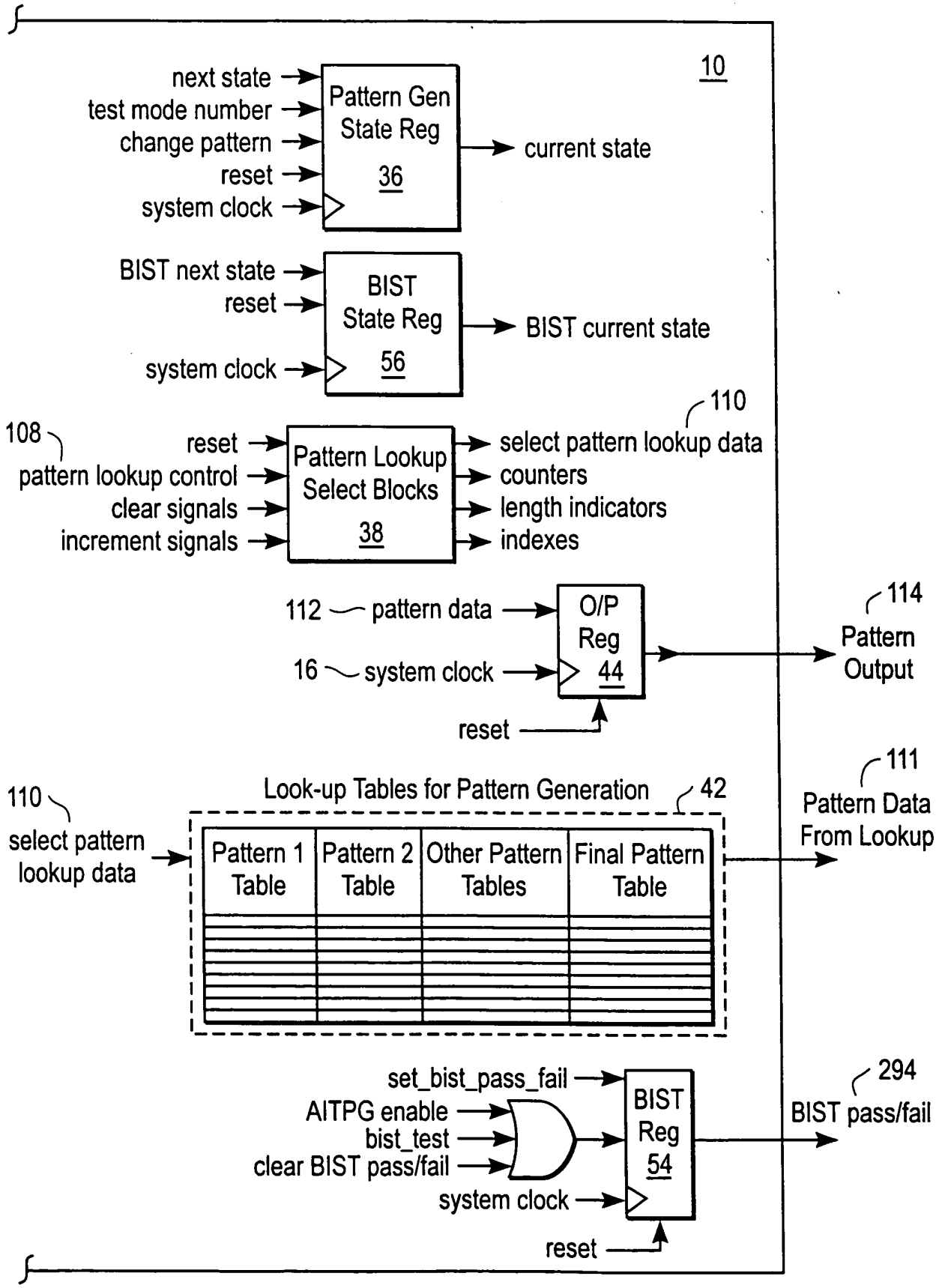
FIG. 1A



← Fig. 1A

FIG. 1B

Fig. 1C →


10
next state
test mode number
change pattern
reset
system clock
Pattern Gen State Reg
36
current state
BIST next state
reset
system clock
BIST State Reg
56
BIST current state
108
110
reset
pattern lookup control
clear signals
increment signals
Pattern Lookup Select Blocks
38
select pattern lookup data
counters
length indicators
indexes
112
pattern data
16
system clock
reset
O/P Reg
44
114
Pattern Output
110
select pattern lookup data
Look-up Tables for Pattern Generation
42
Pattern 1 Table
Pattern 2 Table
Other Pattern Tables
Final Pattern Table
111
Pattern Data From Lookup
set_bist_pass_fail
AITPG enable
bist_test
clear BIST pass/fail
system clock
reset
BIST Reg
54
294
BIST pass/fail

← Fig. 1B

FIG. 1C

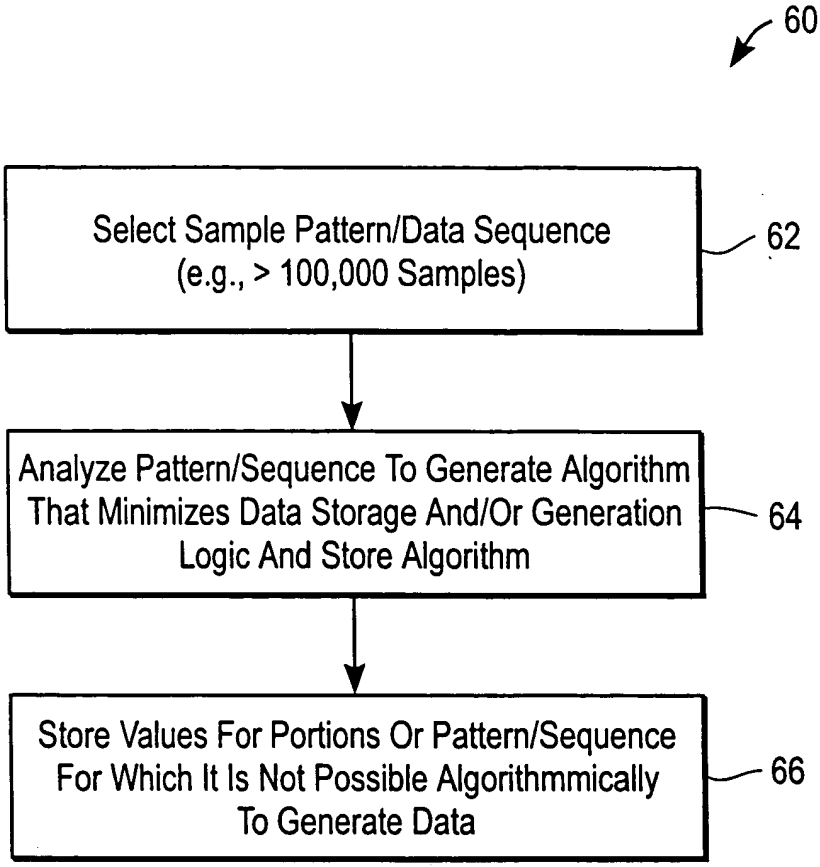

60
Select Sample Pattern/Data Sequence (e.g., > 100,000 Samples)
62
Analyze Pattern/Sequence To Generate Algorithm That Minimizes Data Storage And/Or Generation Logic And Store Algorithm
64
Store Values For Portions Or Pattern/Sequence For Which It Is Not Possible Algorithmmically To Generate Data
66

FIG. 2

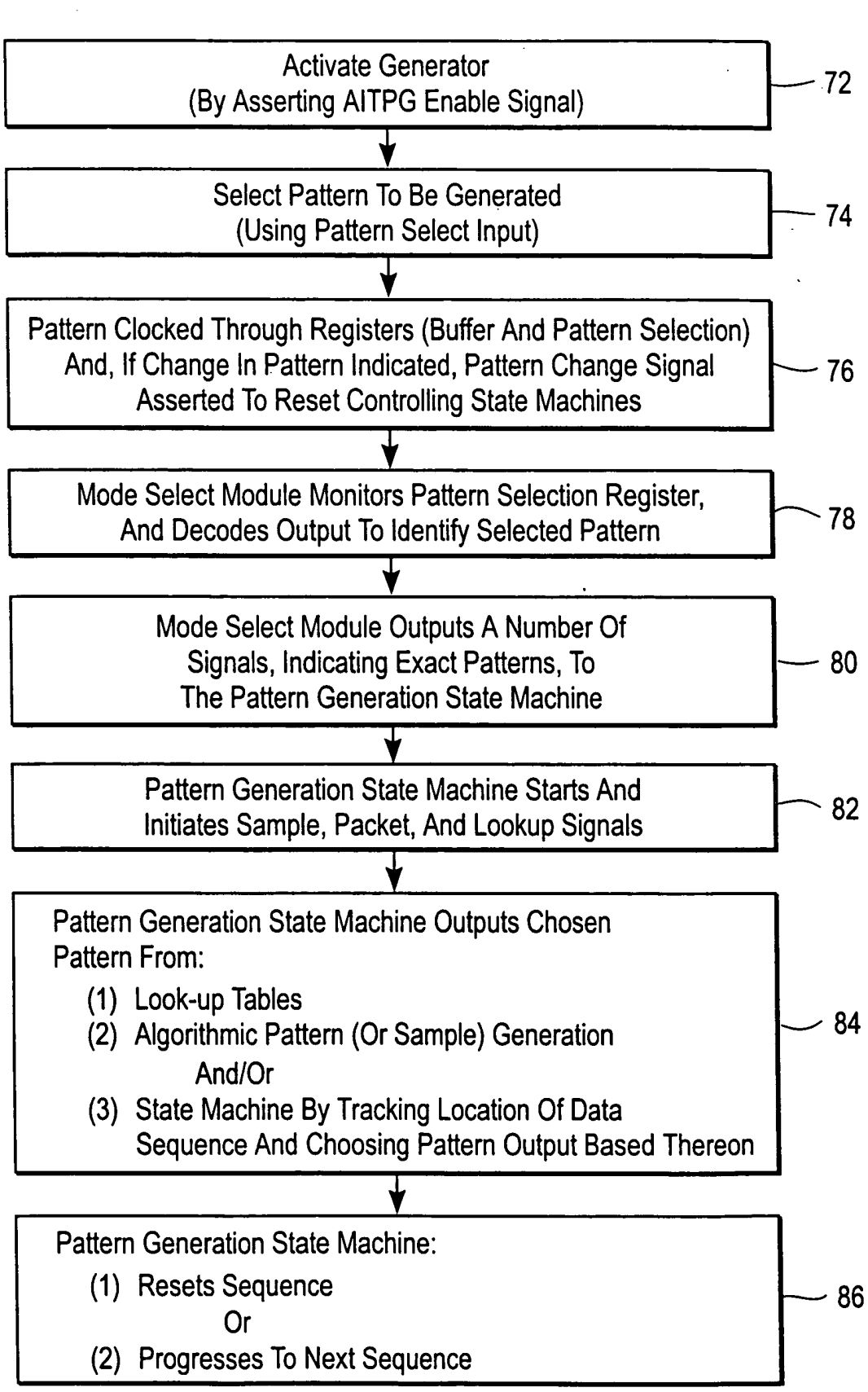

70
Activate Generator
(By Asserting AITPG Enable Signal)
72
Select Pattern To Be Generated
(Using Pattern Select Input)
74
Pattern Clocked Through Registers (Buffer And Pattern Selection)
And, If Change In Pattern Indicated, Pattern Change Signal
Asserted To Reset Controlling State Machines
76
Mode Select Module Monitors Pattern Selection Register,
And Decodes Output To Identify Selected Pattern
78
Mode Select Module Outputs A Number Of
Signals, Indicating Exact Patterns, To
The Pattern Generation State Machine
80
Pattern Generation State Machine Starts And
Initiates Sample, Packet, And Lookup Signals
82
Pattern Generation State Machine Outputs Chosen
Pattern From:
(1) Look-up Tables
(2) Algorithmic Pattern (Or Sample) Generation
And/Or
(3) State Machine By Tracking Location Of Data
Sequence And Choosing Pattern Output Based Thereon
84
Pattern Generation State Machine:
(1) Resets Sequence
Or
(2) Progresses To Next Sequence
86

FIG. 3

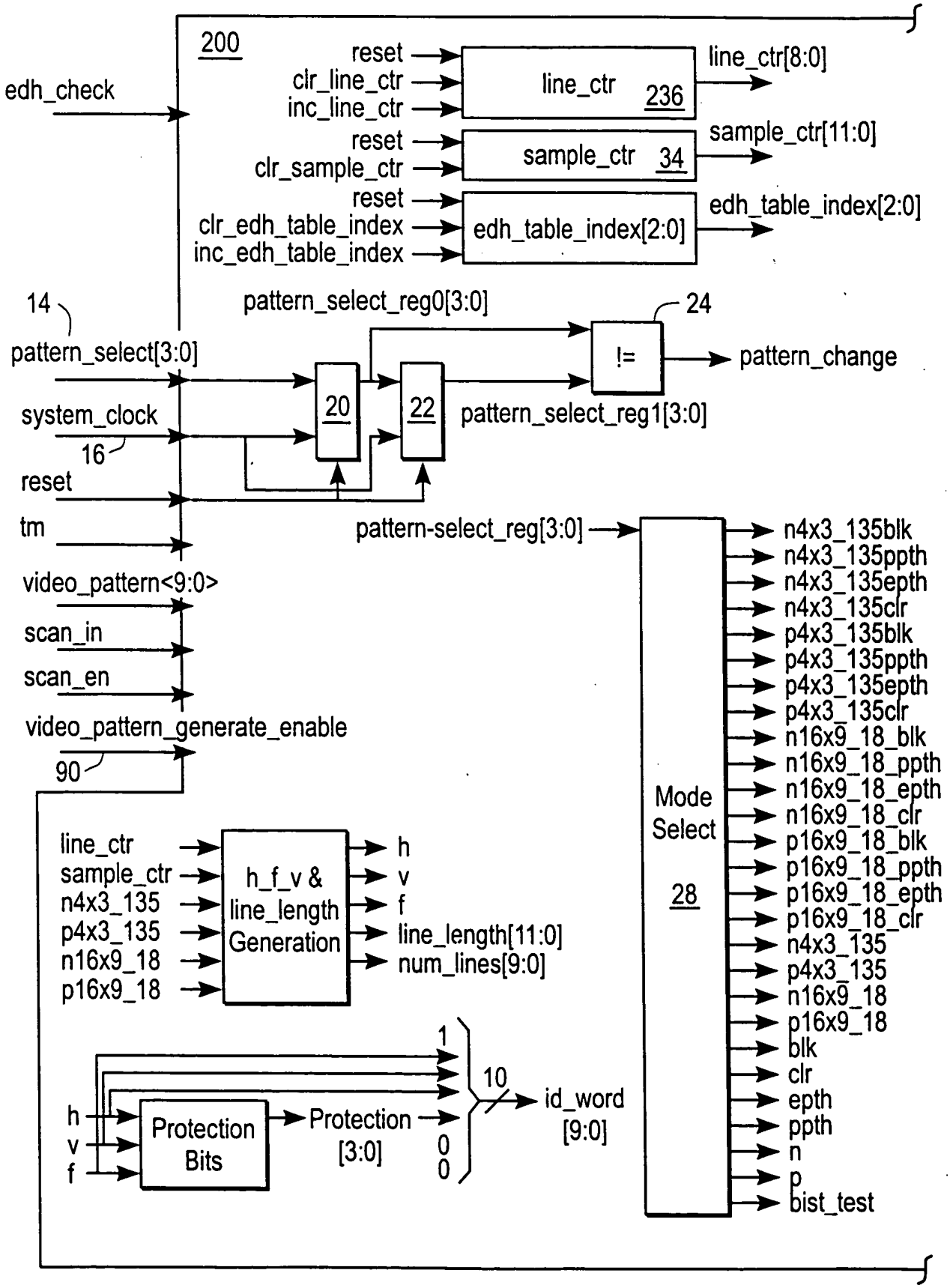
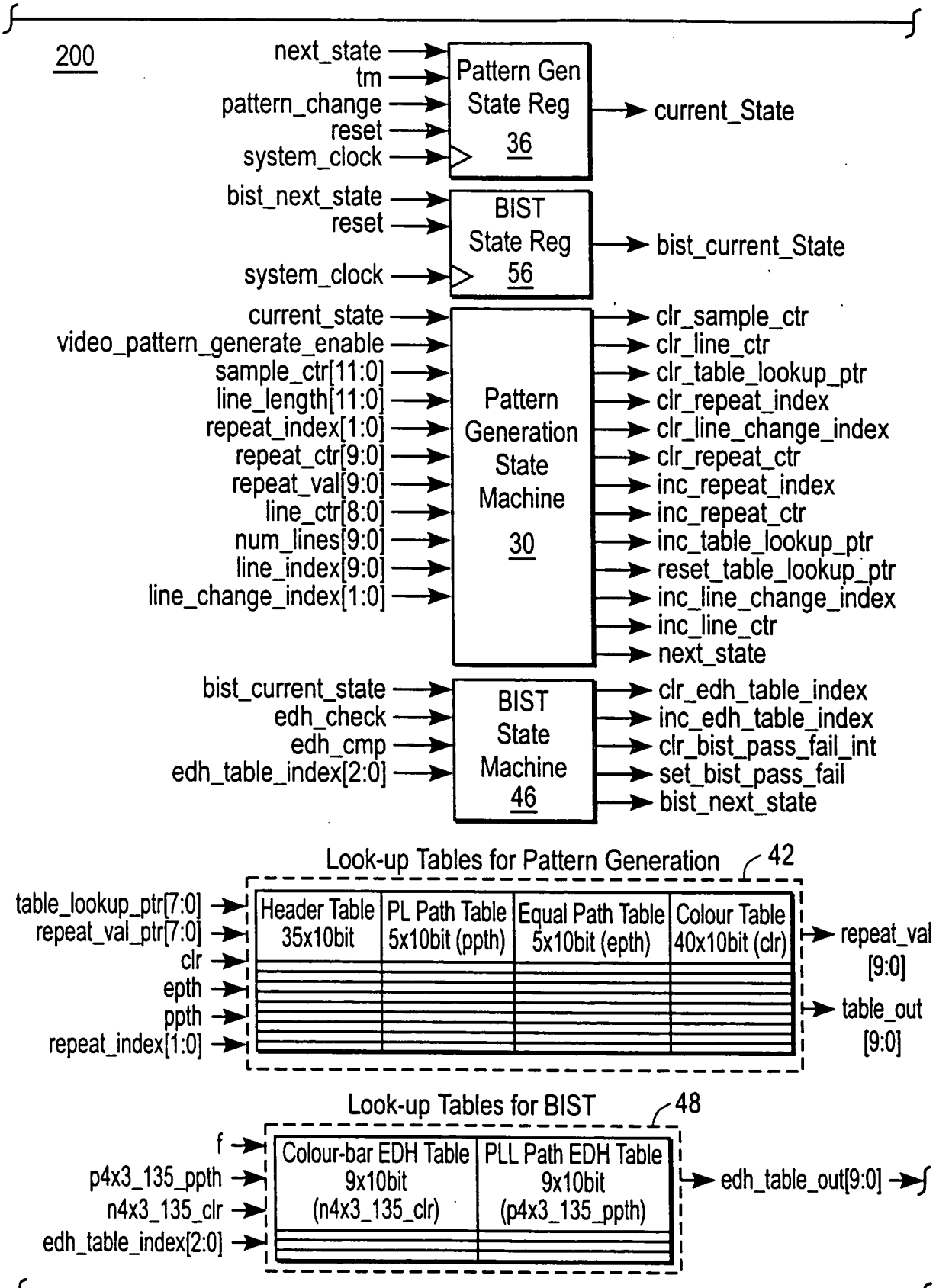

200
edh_check
reset
clr_line_ctr
inc_line_ctr
line_ctr
236
line_ctr[8:0]
reset
clr_sample_ctr
sample_ctr
34
sample_ctr[11:0]
reset
clr_edh_table_index
inc_edh_table_index
edh_table_index[2:0]
edh_table_index[2:0]
14
pattern_select[3:0]
pattern_select_reg0[3:0]
24
!=
pattern_change
system_clock
16
20
22
pattern_select_reg1[3:0]
reset
tm
pattern-select_reg[3:0]
video_pattern<9:0>
scan_in
scan_en
video_pattern_generate_enable
90
line_ctr
sample_ctr
n4x3_135
p4x3_135
n16x9_18
p16x9_18
h_f_v &
line_length
Generation
h
v
f
line_length[11:0]
num_lines[9:0]
1
10
0
0
h
v
f
Protection
Bits
Protection
[3:0]
id_word
[9:0]
Mode
Select
28
n4x3_135blk
n4x3_135ppth
n4x3_135epth
n4x3_135clr
p4x3_135blk
p4x3_135ppth
p4x3_135epth
p4x3_135clr
n16x9_18_blk
n16x9_18_ppth
n16x9_18_epth
n16x9_18_clr
p16x9_18_blk
p16x9_18_ppth
p16x9_18_epth
p16x9_18_clr
n4x3_135
p4x3_135
n16x9_18
p16x9_18
blk
clr
epth
ppth
n
p
bist_test

FIG. 4A

Fig. 4B →



← Fig. 4A

FIG. 4B

Fig. 4C →

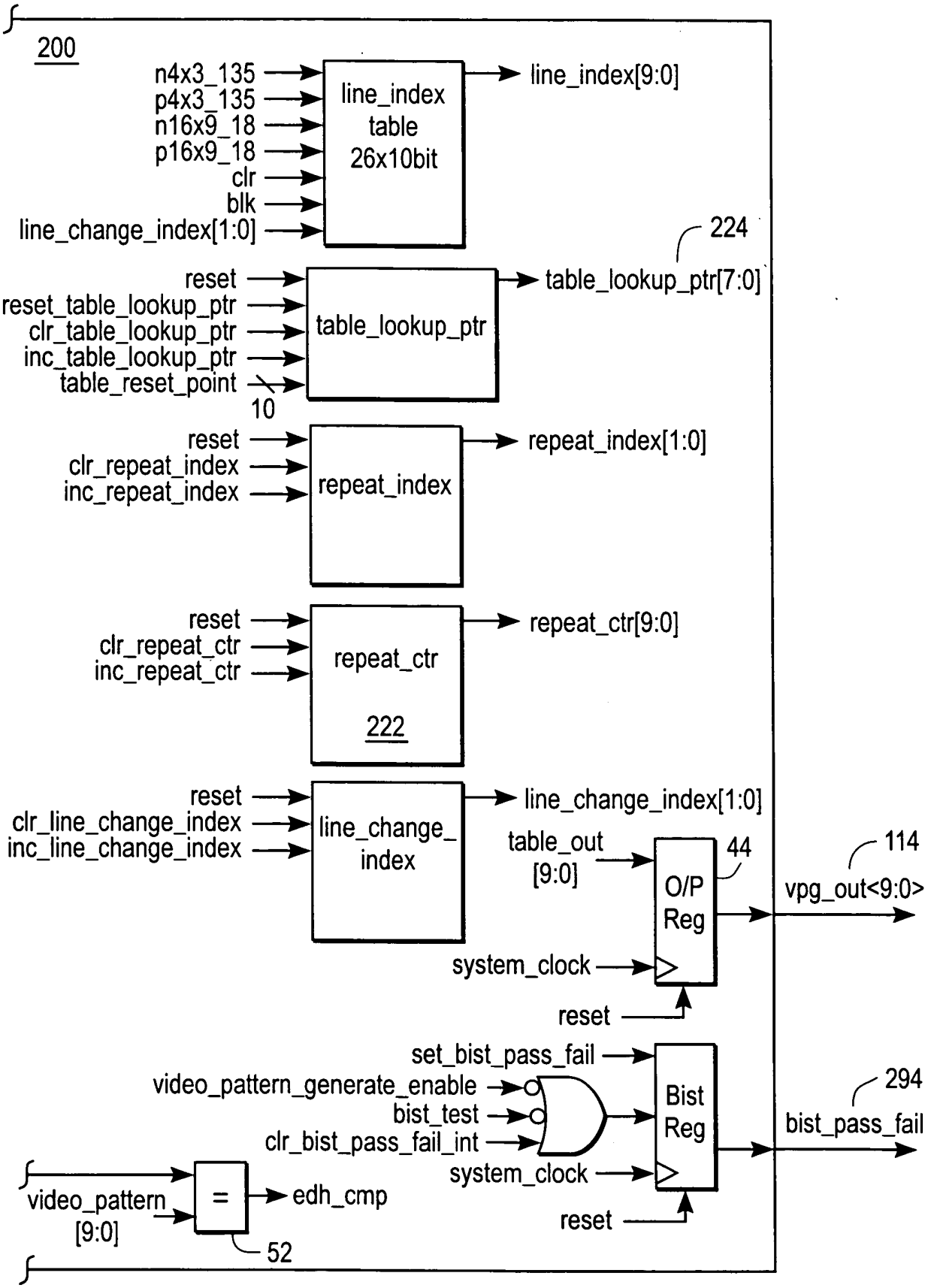

200
n4x3_135
p4x3_135
n16x9_18
p16x9_18
clr
blk
line_change_index[1:0]
line_index table 26x10bit
line_index[9:0]
224
reset
reset_table_lookup_ptr
clr_table_lookup_ptr
inc_table_lookup_ptr
table_reset_point
10
table_lookup_ptr
table_lookup_ptr[7:0]
reset
clr_repeat_index
inc_repeat_index
repeat_index
repeat_index[1:0]
reset
clr_repeat_ctr
inc_repeat_ctr
repeat_ctr
222
repeat_ctr[9:0]
reset
clr_line_change_index
inc_line_change_index
line_change_ index
line_change_index[1:0]
table_out [9:0]
44
O/P Reg
114
vpg_out<9:0>
system_clock
reset
set_bist_pass_fail
video_pattern_generate_enable
bist_test
clr_bist_pass_fail_int
system_clock
reset
Bist Reg
294
bist_pass_fail
video_pattern [9:0]
=
edh_cmp
52
Fig. 4B

FIG. 4C

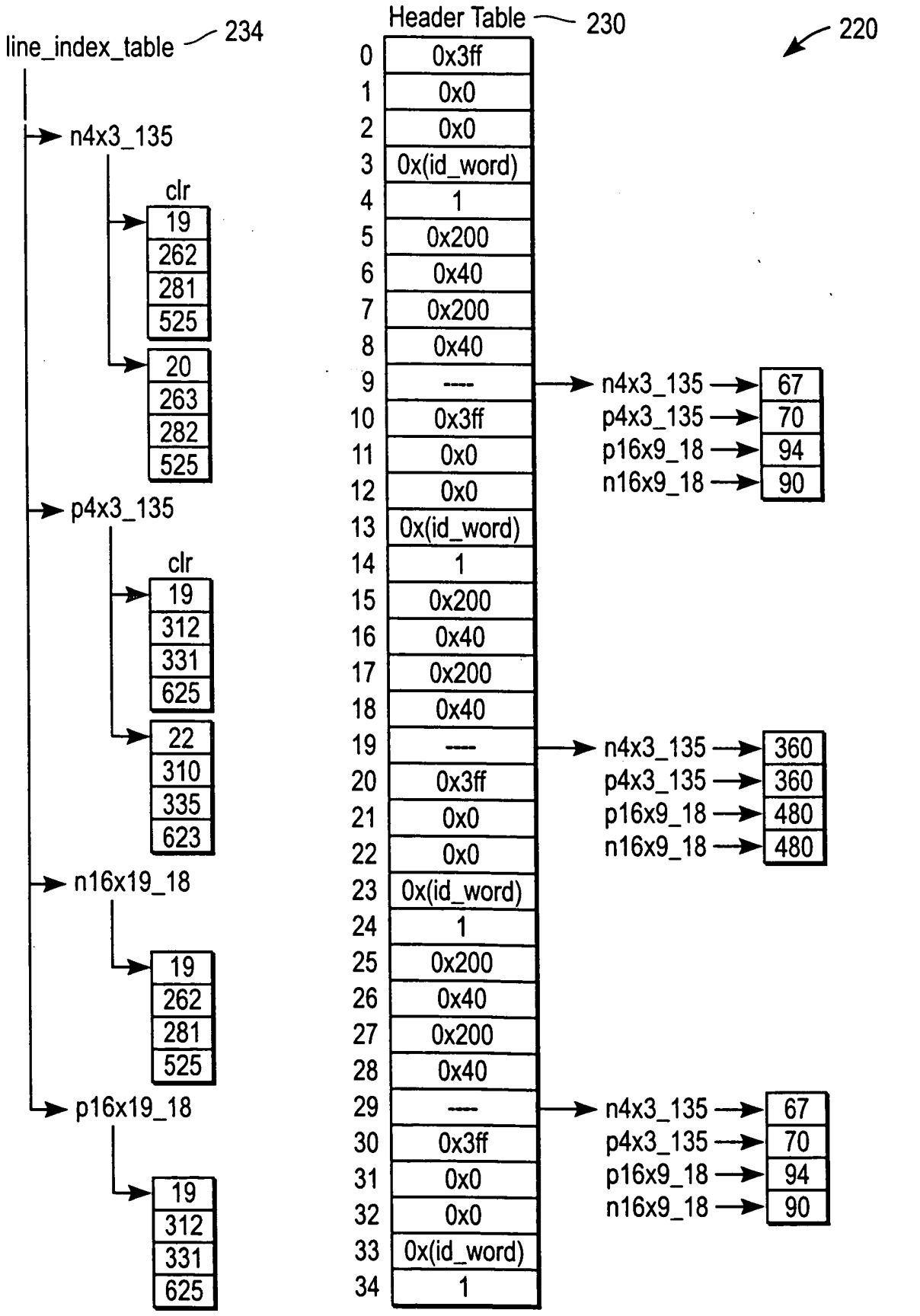
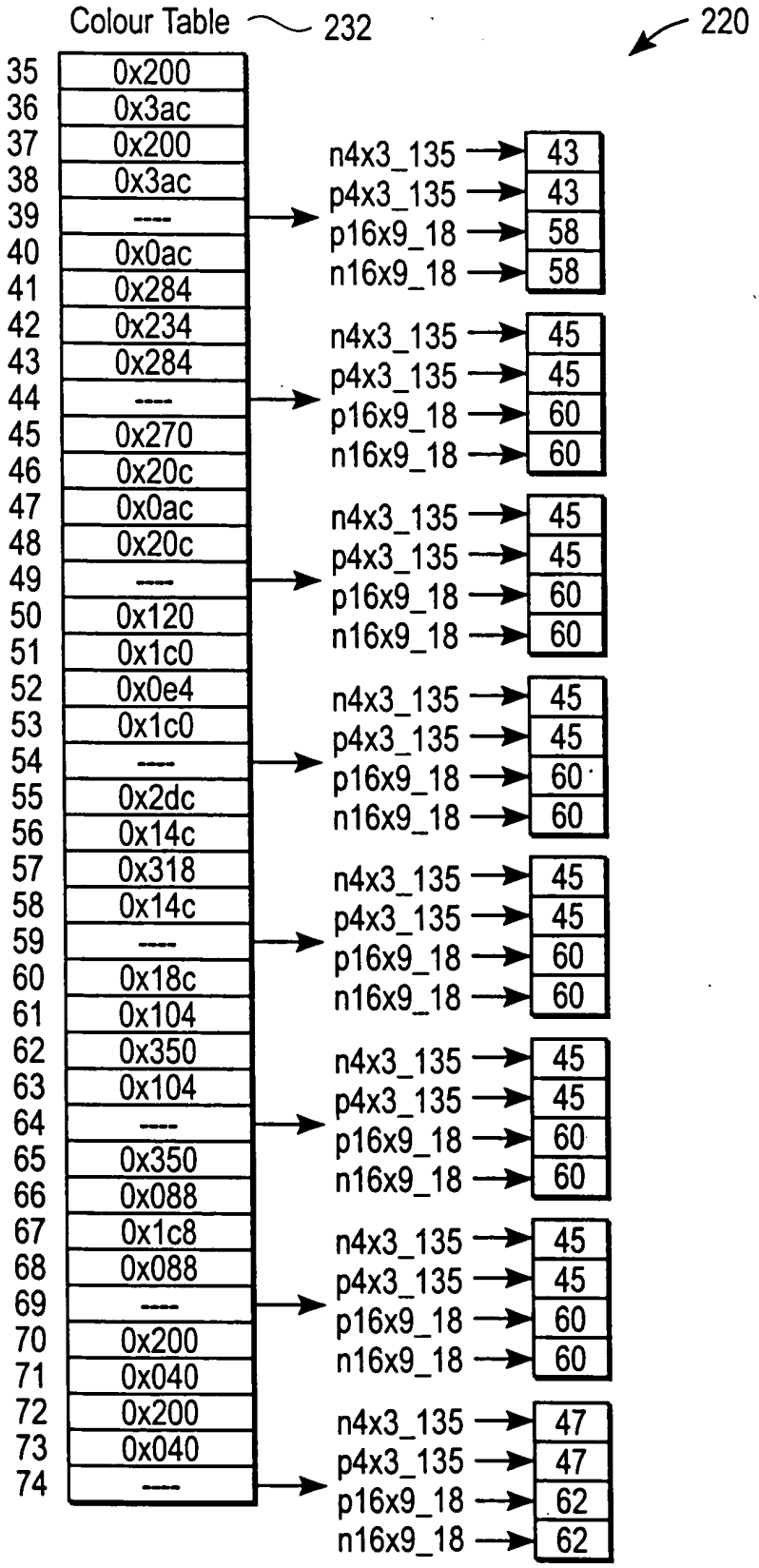

line_index_table
234
n4x3_135
clr
19
262
281
525
20
263
282
525
p4x3_135
clr
19
312
331
625
22
310
335
623
n16x19_18
19
262
281
525
p16x19_18
19
312
331
625
Header Table
230
220
0 0x3ff
1 0x0
2 0x0
3 0x(id_word)
4 1
5 0x200
6 0x40
7 0x200
8 0x40
9 ----
10 0x3ff
11 0x0
12 0x0
13 0x(id_word)
14 1
15 0x200
16 0x40
17 0x200
18 0x40
19 ----
20 0x3ff
21 0x0
22 0x0
23 0x(id_word)
24 1
25 0x200
26 0x40
27 0x200
28 0x40
29 ----
30 0x3ff
31 0x0
32 0x0
33 0x(id_word)
34 1
n4x3_135 67
p4x3_135 70
p16x9_18 94
n16x9_18 90
n4x3_135 360
p4x3_135 360
p16x9_18 480
n16x9_18 480
n4x3_135 67
p4x3_135 70
p16x9_18 94
n16x9_18 90

FIG. 5A

Fig. 5B →



← Fig. 5A

FIG. 5B

Fig. 5C →

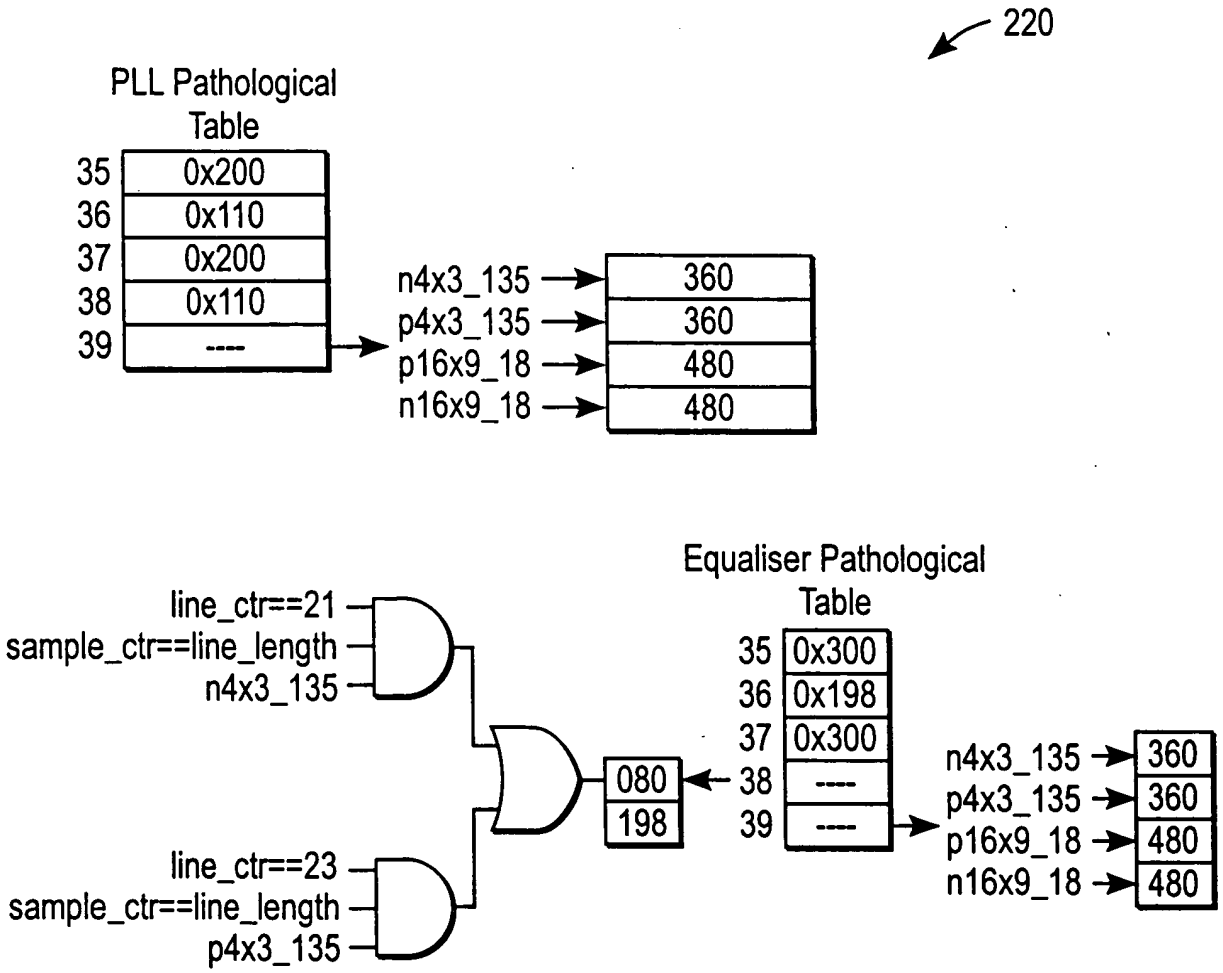

220
PLL Pathological Table
35 0x200
36 0x110
37 0x200
38 0x110
39 ----
n4x3_135 → 360
p4x3_135 → 360
p16x9_18 → 480
n16x9_18 → 480
Equaliser Pathological Table
35 0x300
36 0x198
37 0x300
38 ----
39 ----
080
198
line_ctr==21
sample_ctr==line_length
n4x3_135
line_ctr==23
sample_ctr==line_length
p4x3_135
n4x3_135 → 360
p4x3_135 → 360
p16x9_18 → 480
n16x9_18 → 480

FIG. 5C

← Fig. 5B

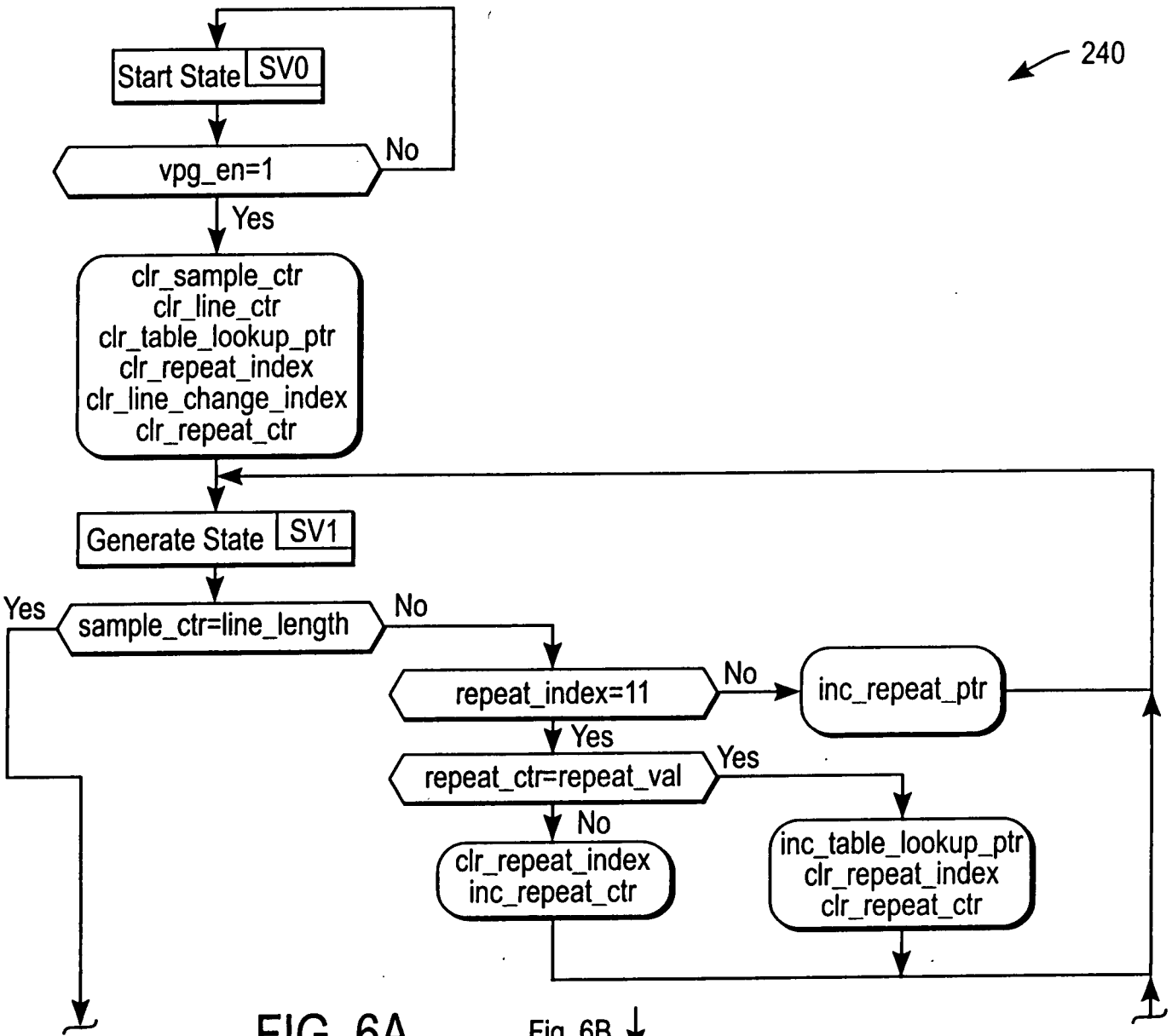

240
Start State SV0
vpg_en=1
No
Yes
clr_sample_ctr
clr_line_ctr
clr_table_lookup_ptr
clr_repeat_index
clr_line_change_index
clr_repeat_ctr
Generate State SV1
Yes
sample_ctr=line_length
No
repeat_index=11
No
inc_repeat_ptr
Yes
repeat_ctr=repeat_val
Yes
No
clr_repeat_index
inc_repeat_ctr
inc_table_lookup_ptr
clr_repeat_index
clr_repeat_ctr

FIG. 6A

Fig. 6B

Fig. 6A

240

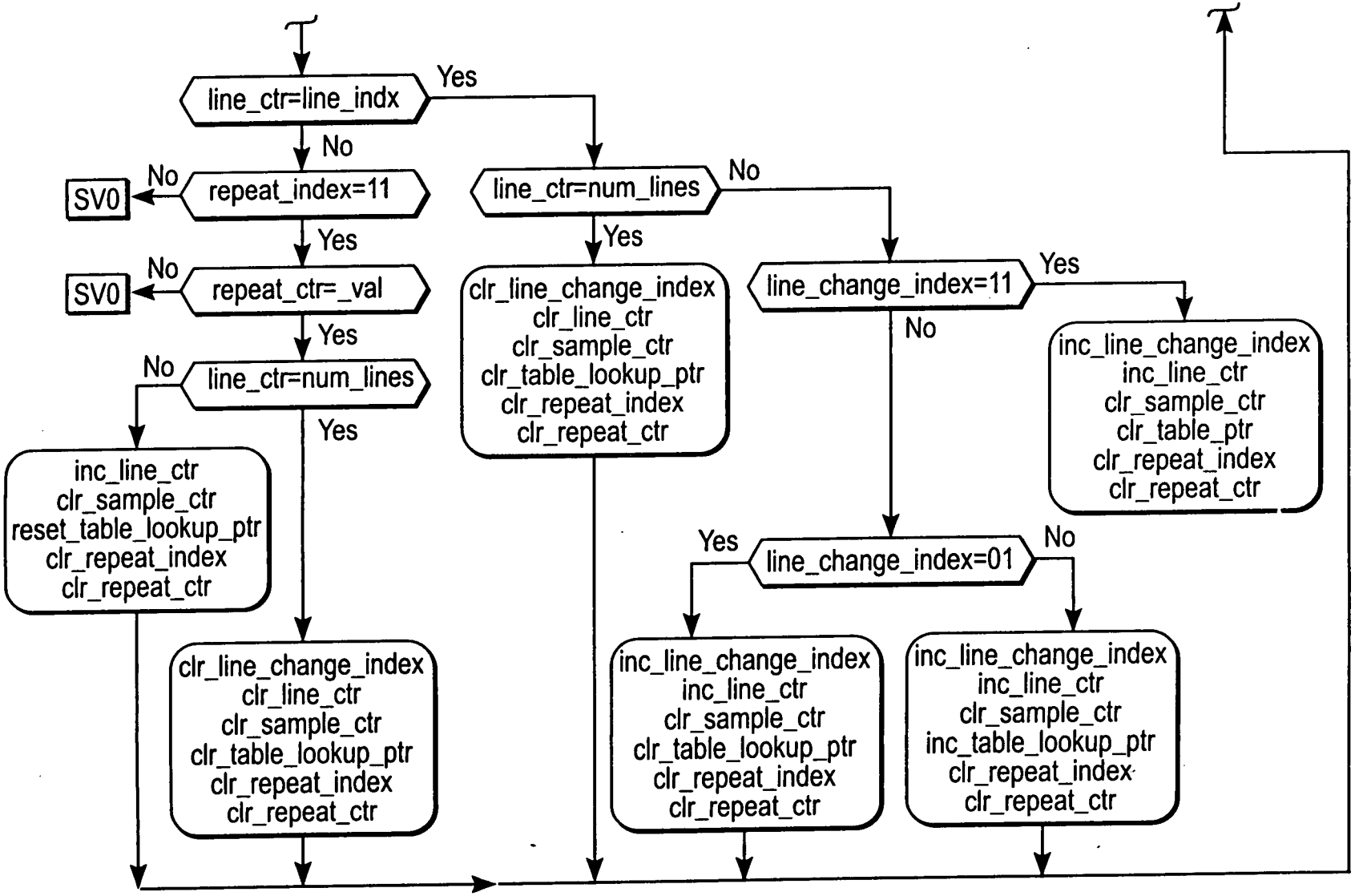


FIG. 6B

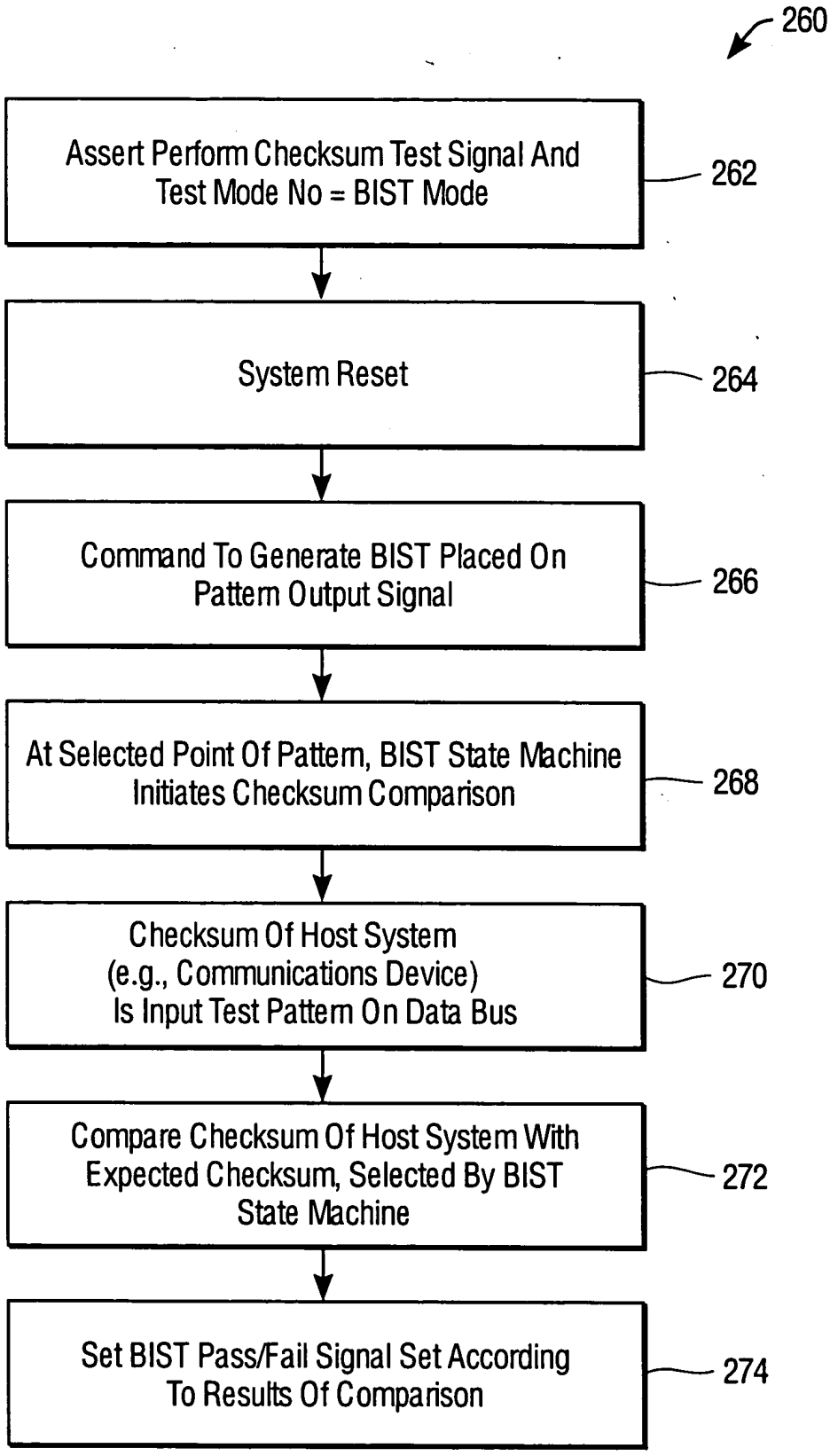

260
Assert Perform Checksum Test Signal And Test Mode No = BIST Mode
262
System Reset
264
Command To Generate BIST Placed On Pattern Output Signal
266
At Selected Point Of Pattern, BIST State Machine Initiates Checksum Comparison
268
Checksum Of Host System (e.g., Communications Device) Is Input Test Pattern On Data Bus
270
Compare Checksum Of Host System With Expected Checksum, Selected By BIST State Machine
272
Set BIST Pass/Fail Signal Set According To Results Of Comparison
274

FIG. 7

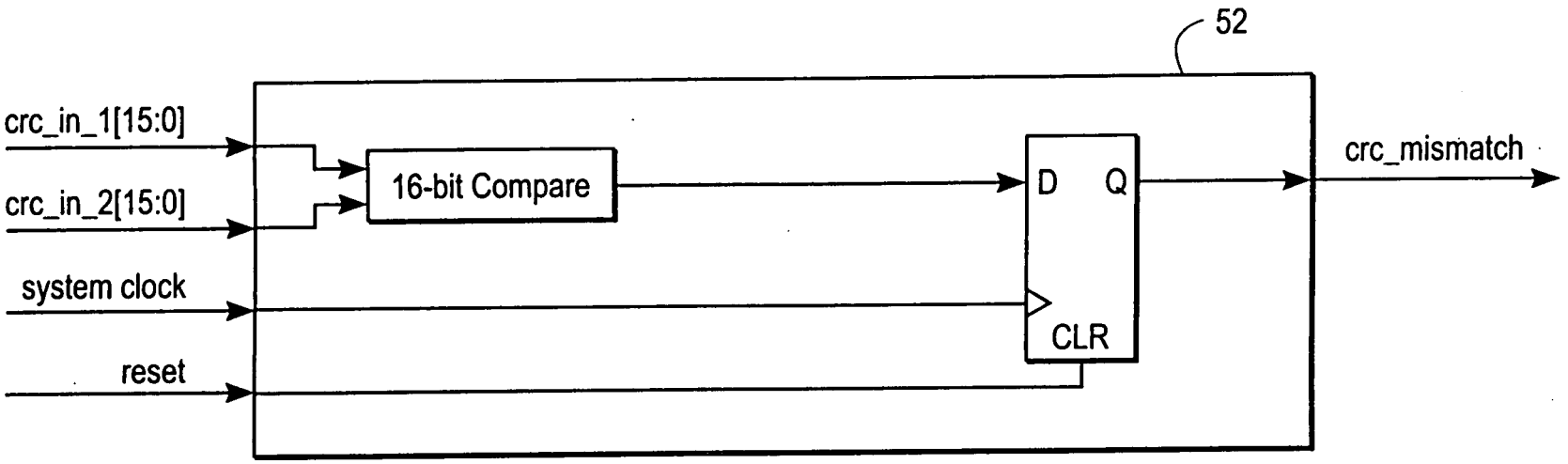

52
crc_in_1[15:0]
crc_in_2[15:0]
system clock
reset
16-bit Compare
D
Q
CLR
crc_mismatch

FIG. 8

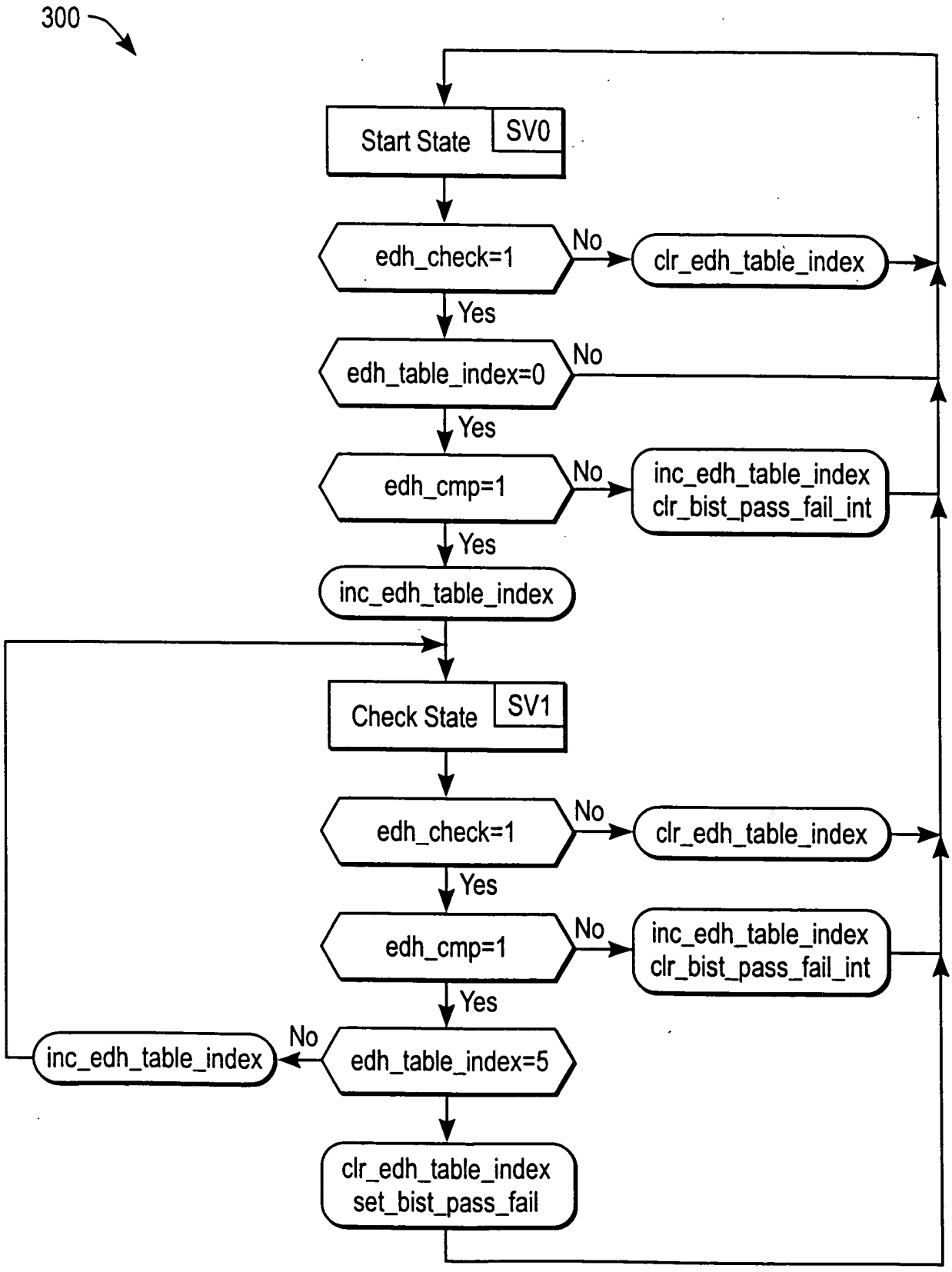

300
Start State
SV0
edh_check=1
No
clr_edh_table_index
Yes
edh_table_index=0
No
Yes
edh_cmp=1
No
inc_edh_table_index
clr_bist_pass_fail_int
Yes
inc_edh_table_index
Check State
SV1
edh_check=1
No
clr_edh_table_index
Yes
edh_cmp=1
No
inc_edh_table_index
clr_bist_pass_fail_int
Yes
No
edh_table_index=5
inc_edh_table_index
clr_edh_table_index
set_bist_pass_fail

FIG. 9

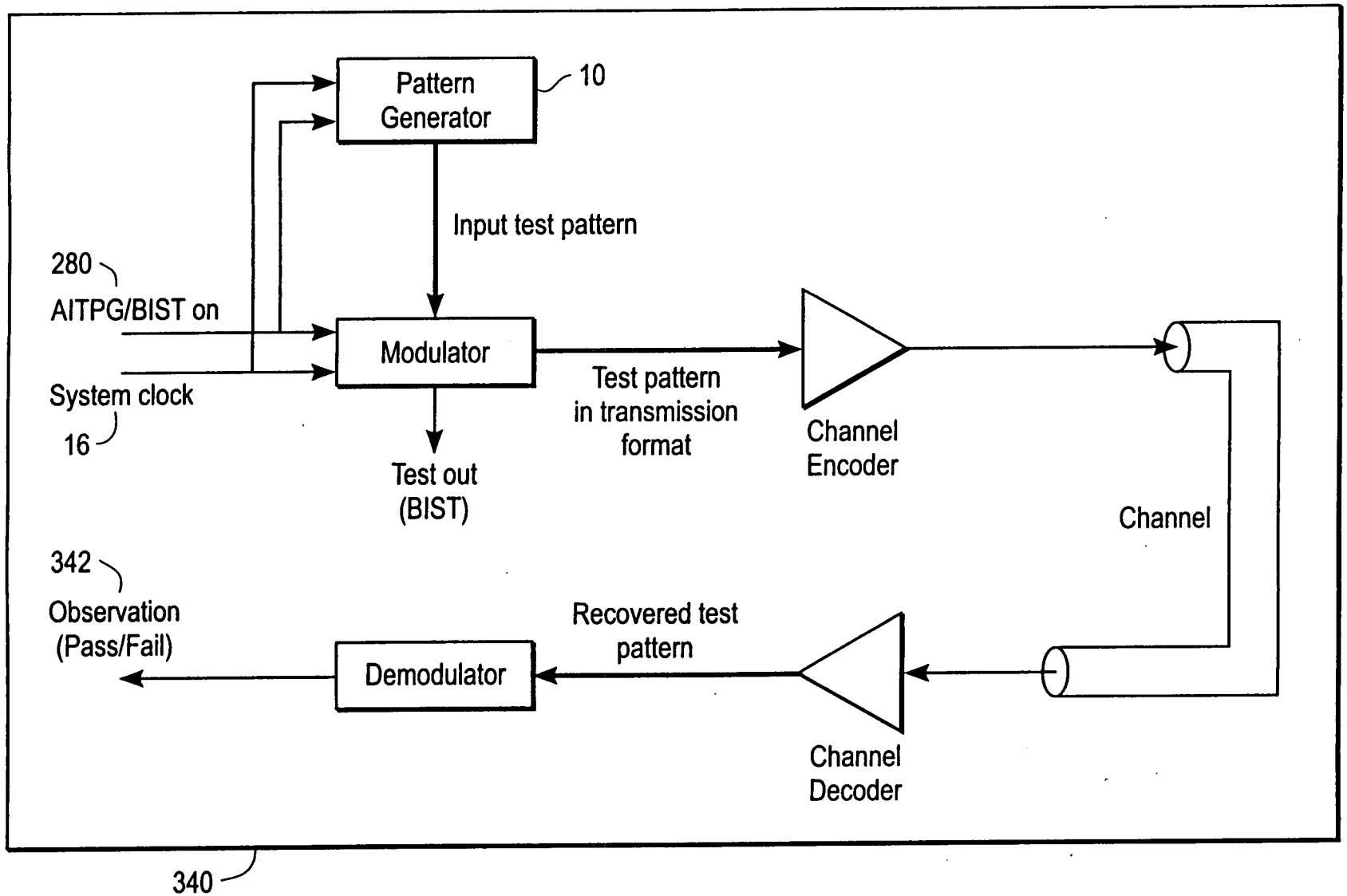

Pattern Generator
10
Input test pattern
280
AITPG/BIST on
Modulator
System clock
16
Test out (BIST)
Test pattern in transmission format
Channel Encoder
Channel
342
Observation (Pass/Fail)
Demodulator
Recovered test pattern
Channel Decoder
340

FIG. 10

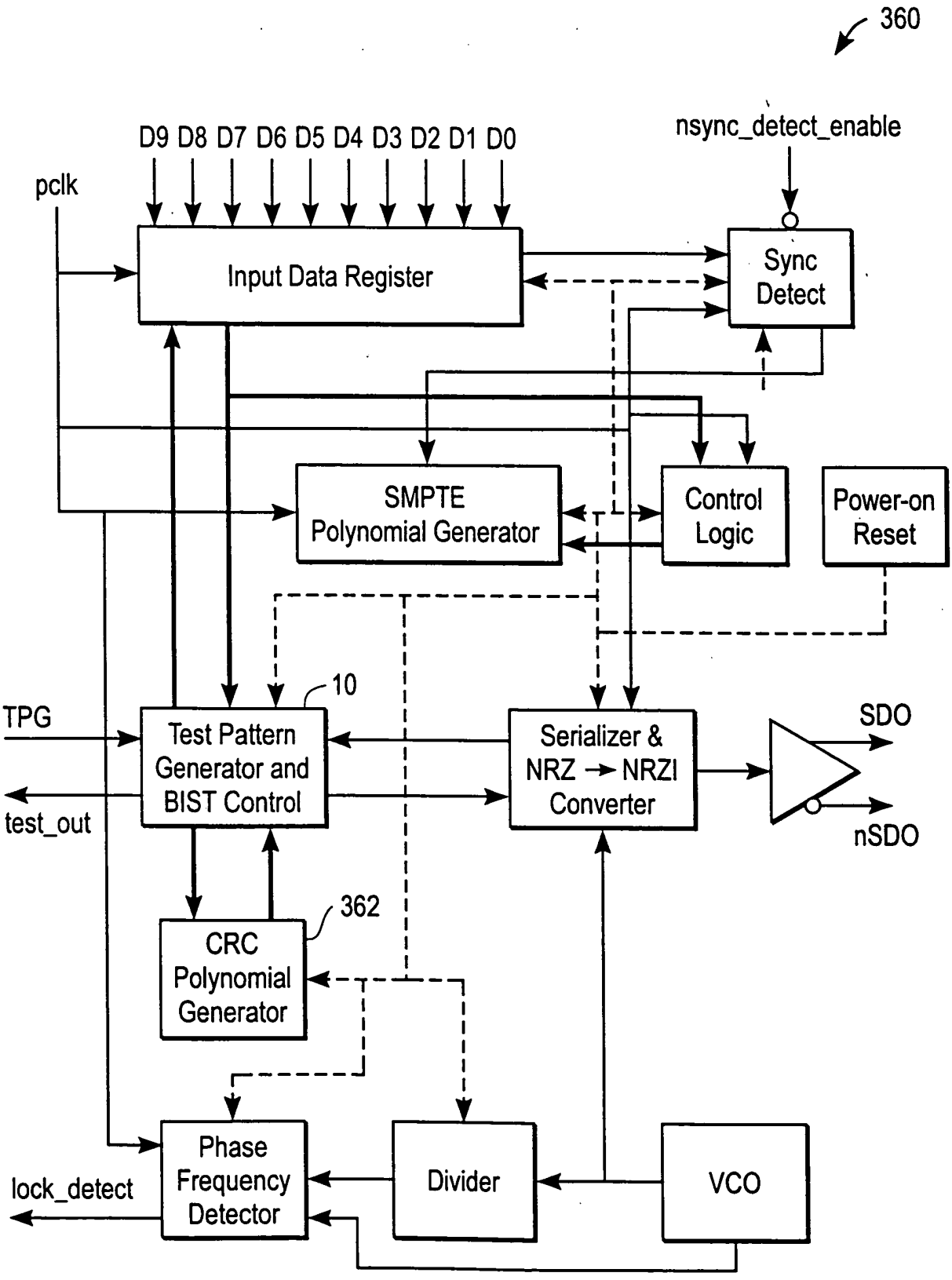

360
D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
nsync_detect_enable
pclk
Input Data Register
Sync Detect
SMPTE Polynomial Generator
Control Logic
Power-on Reset
10
TPG
Test Pattern Generator and BIST Control
Serializer & NRZ → NRZI Converter
SDO
nSDO
test_out
362
CRC Polynomial Generator
Phase Frequency Detector
Divider
VCO
lock_detect

FIG. 11